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TFT LCD Approval Specification

MODEL NO.: V420H1 – LE1

Customer: _____

Approved by:_____

Note:

Approved By	TV Product Marketing & Management Div
	Chao-Chun Chung

Reviewed By	QA Dept.	Product Development Div.
	Hsin-Nan Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	CY Chang	HT Hung

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Oct 13,09'	All	All	Approval Specification was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420 H1- LE1 is a 42" TFT Liquid Crystal Display module with LED Backlight and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 1.07G colors (8-bit +FRC). The converter module for backlight is built-in.

1.2 FEATURES

-High brightness (450 nits)
- Ultra-high contrast ratio (4000:1)
- Faster response time (gray to gray average 4.5 ms)
- High color saturation NTSC 72%
- Ultra wide viewing angle: 176(H)/176(V) (CR≥20) with Super MVA technology
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
-Optimized response time for 100/120 Hz frame rate

1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	930.24 (H) x 523.26 (V) (42" diagonal)	mm	(1)
Bezel Opening Area	937.24 (H) x 530.26 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	1.07G	color	
Display Operation Mode	Transmissive mode / Normally Black	-	
Surface Treatment	Anti-Glare Coating (Haze 11%) Hard Coating (3H)	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	983	-	mm	(1)
	Vertical(V)	-	576	-	mm	(1)
	Depth(D)	10	11	12	mm	
	Depth(D)		26.8		mm	To converter cover
Weight			8600			

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

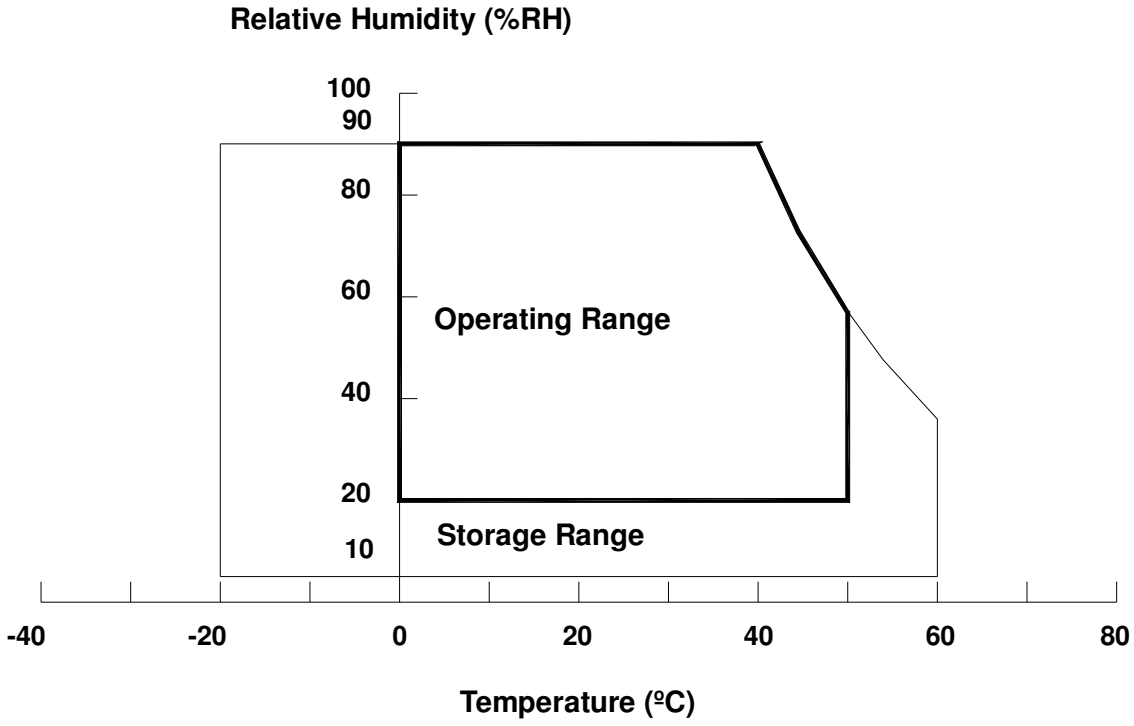
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



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2.2 Package storage

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

(b)The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.5	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V_W	Ta = 25 ℃	-	-	60	V_{RMS}	
Converter Input Voltage	V_{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating condition.

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3. ELECTRICAL CHARACTERISTICS

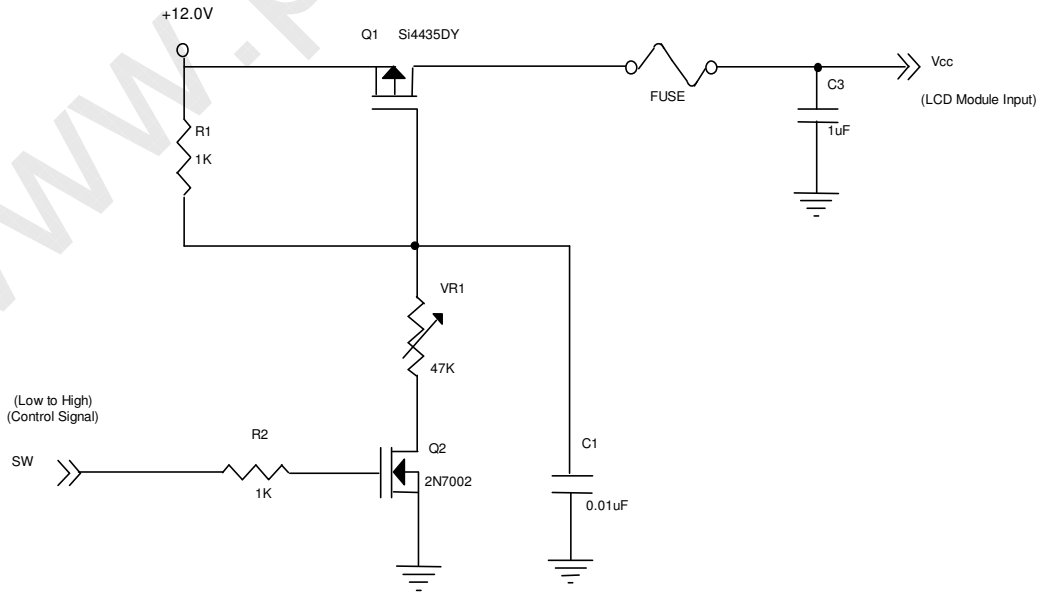
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	5.4	A	(2)
Power Supply Current	White Pattern	-	-	1.3	1.69	A	(3)
	Horizontal Stripe	-	-	1.32	1.716	A	
	Black Pattern	-	-	0.83	-	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



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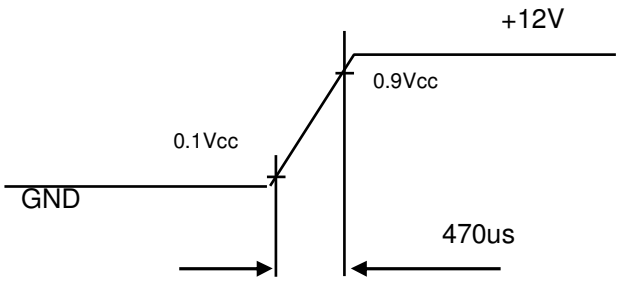
Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc =12V, Ta = 25 ± 2 ºC, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

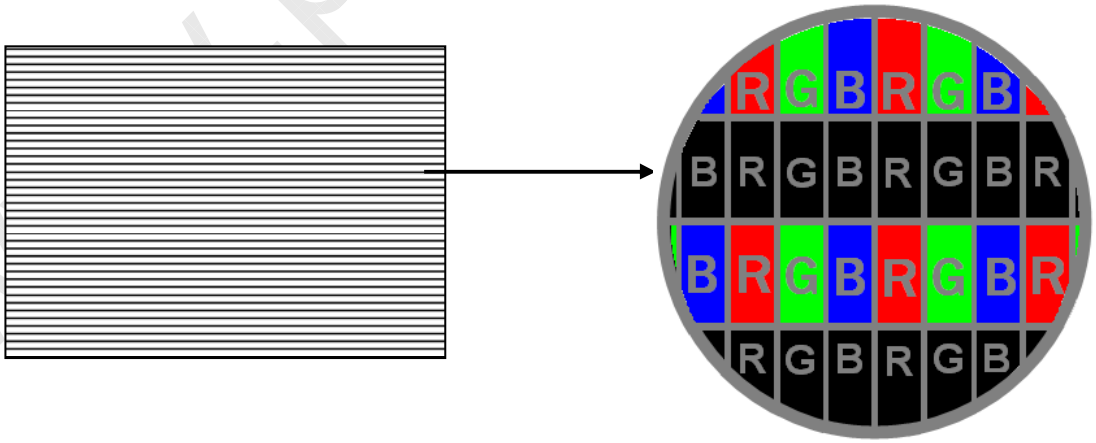
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Horizontal Pattern



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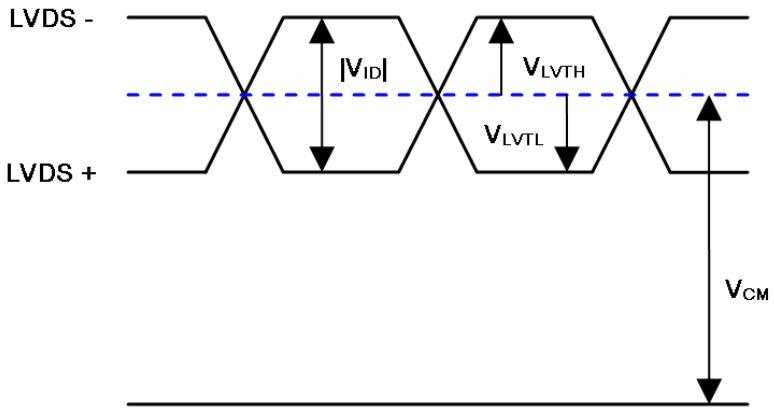
Note (4) The LVDS input characteristics are as follows:



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3.2 BACKLIGHT CONVERTER UNIT

3.2.1 LED LIGHT BARCHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Light Bar Voltage	V_W	-	-	44.2	V_{RMS}	I_L =60 mA
LED Forward Voltage	V_f	3.0	3.2	3.4	V_{RMS}	I_L =60mA
LED Current	I_L	56.4	60	63.6	mA	

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	84	92.4	W	
Converter Input Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Converter Input Current	I_{BL}	-	3.5	-	A	
Dimming Frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	5	-	%	

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

External dimming: 150Hz~170Hz, duty ratio: 5%~100%

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	3.15	—	3.45	V	maximum duty ratio
	MIN		—	—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on
	LO		—	0	—	0.8	V	Duty off
Status Signal	HI	Status	—	3.0	3.3	3.6	V	Normal
	LO		—	0	—	0.8	V	Abnormal
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V_{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		TPWMR	—	—	—	50	us	
PWM Signal Falling Time		TPWMF	—	—	—	50	us	

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Input Impedance	Rin	–	1	–	–	MΩ	
PWM Delay Time	TPWM	–	100	–	–	ms	
BLON Delay Time	T_{on}	–	300	–	–	ms	
	T_{on1}	–	300	–	–	ms	
BLON Off Time	Toff	–	300	–	–	ms	

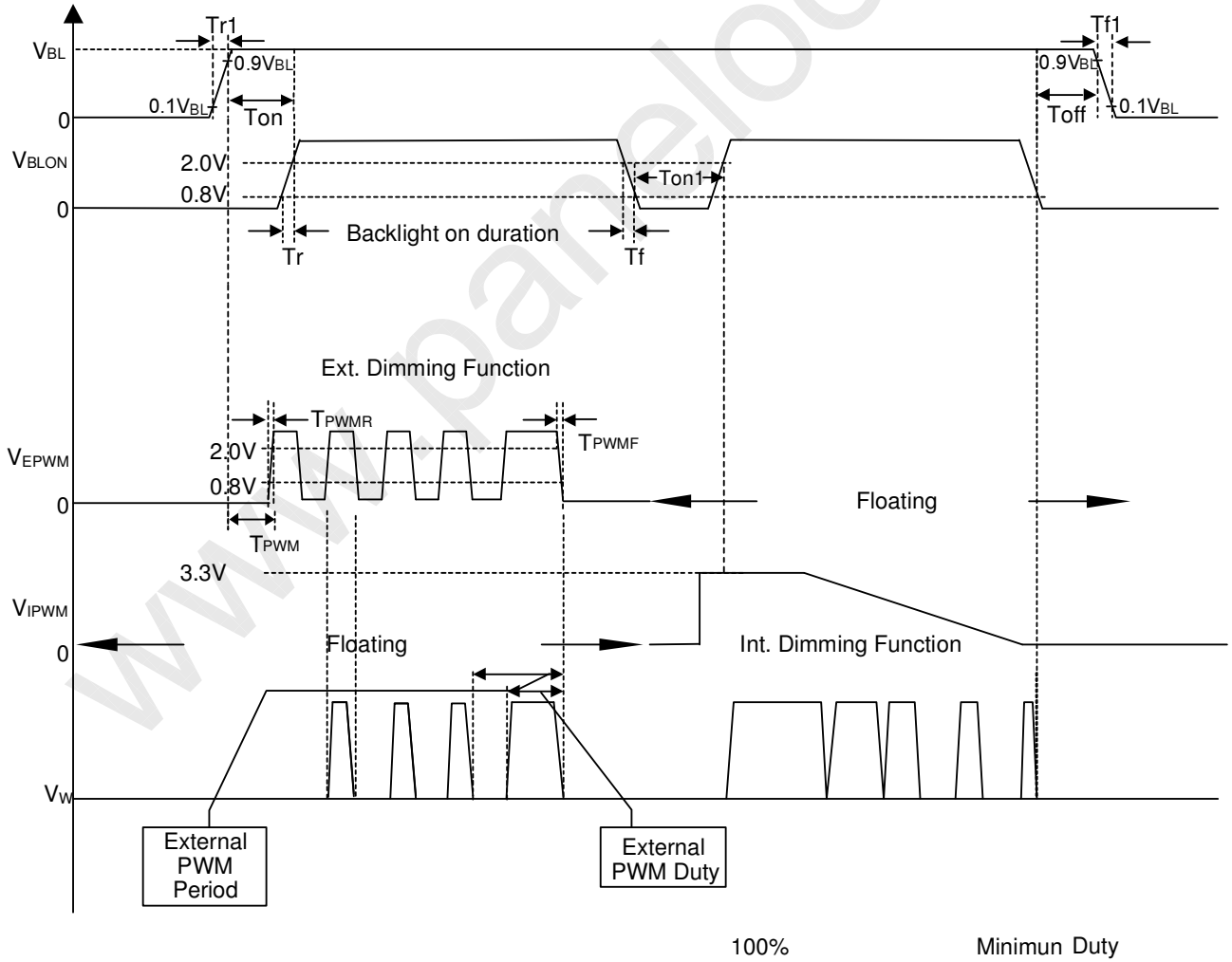
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



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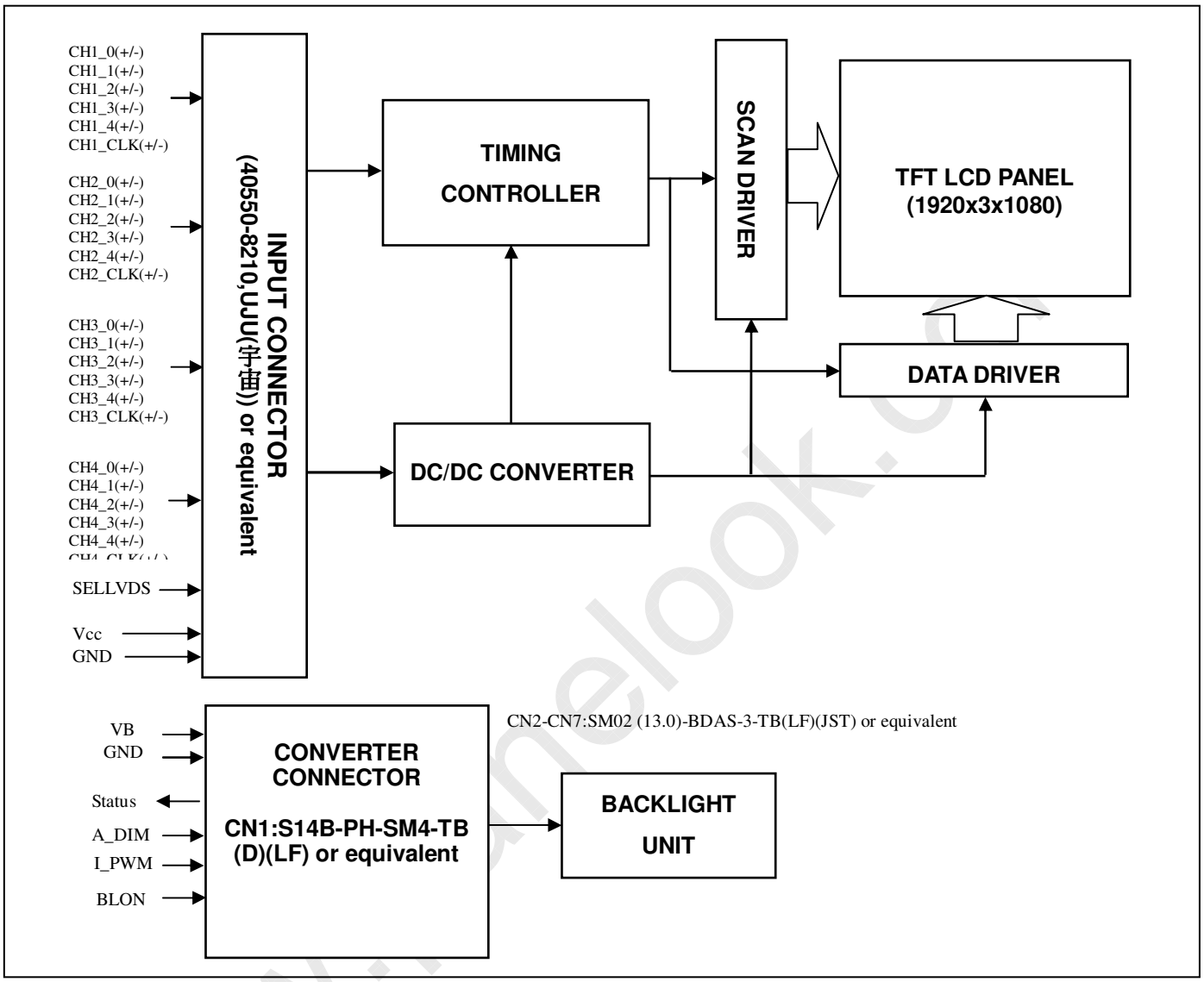
4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



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5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF2 Connector Pin Assignment (FI-RE41S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3_0N	Third Pixel Negative LVDS differential data input. Channel 0	(4)
11	CH3_0P	Third Pixel Positive LVDS differential data input. Channel 0	
12	CH3_1N	Third Pixel Negative LVDS differential data input. Channel 1	
13	CH3_1P	Third Pixel Positive LVDS differential data input. Channel 1	
14	CH3_2N	Third Pixel Negative LVDS differential data input. Channel 2	
15	CH3_2P	Third Pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	CH3_CLKN	Third Pixel Negative LVDS differential clock input.	
18	CH3_CLKP	Third Pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3_3N	Third Pixel Negative LVDS differential data input. Channel 3	(4)
21	CH3_3P	Third Pixel Positive LVDS differential data input. Channel 3	
22	CH3_4N	Third Pixel Negative LVDS differential data input. Channel 4	
23	CH3_4P	Third Pixel Positive LVDS differential data input. Channel 4	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	CH4_0N	Fourth Pixel Negative LVDS differential data input. Channel 0	(4)
27	CH4_0P	Fourth Pixel Positive LVDS differential data input. Channel 0	
28	CH4_1N	Fourth Pixel Negative LVDS differential data input. Channel 1	
29	CH4_1P	Fourth Pixel Positive LVDS differential data input. Channel 1	
30	CH4_2N	Fourth Pixel Negative LVDS differential data input. Channel 2	
31	CH4_2P	Fourth Pixel Positive LVDS differential data input. Channel 2	
32	GND	Ground	
33	CH4_CLKN	Fourth Pixel Negative LVDS differential clock input.	
34	CH4_CLKP	Fourth Pixel Positive LVDS differential clock input.	
35	GND	Ground	(4)
36	CH4_3N	Fourth Pixel Negative LVDS differential data input. Channel 3	
37	CH4_3P	Fourth Pixel Positive LVDS differential data input. Channel 3	
38	CH4_4N	Fourth Pixel Negative LVDS differential data input. Channel 4	
39	CH4_4P	Fourth Pixel Positive LVDS differential data input. Channel 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	

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CNF1 Connector Pin Assignment (FI-RE51S-HF (JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	ODSEL	Overdrive Lookup Table Selection	(3)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS data format Selection	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	CH1_0N	First Pixel Negative LVDS differential data input. Channel 0	(4)
13	CH1_0P	First Pixel Positive LVDS differential data input. Channel 0	
14	CH1_1N	First Pixel Negative LVDS differential data input. Channel 1	
15	CH1_1P	First Pixel Positive LVDS differential data input. Channel 1	
16	CH1_2N	First Pixel Negative LVDS differential data input. Channel 2	
17	CH1_2P	First Pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	CH1_CLKN	First Pixel Negative LVDS differential clock input.	
20	CH1_CLKP	First Pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1_3N	First Pixel Negative LVDS differential data input. Channel 3	(4)
23	CH1_3P	First Pixel Positive LVDS differential data input. Channel 3	
24	CH1_4N	First Pixel Negative LVDS differential data input. Channel 4	
25	CH1_4P	First Pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	
28	CH2_0N	Second Pixel Negative LVDS differential data input. Channel 0	(4)
29	CH2_0P	Second Pixel Positive LVDS differential data input. Channel 0	
30	CH2_1N	Second Pixel Negative LVDS differential data input. Channel 1	
31	CH2_1P	Second Pixel Positive LVDS differential data input. Channel 1	
32	CH2_2N	Second Pixel Negative LVDS differential data input. Channel 2	
33	CH2_2P	Second Pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	CH2_CLKN	Second Pixel Negative LVDS differential clock input.	
36	CH2_CLKP	Second Pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2_3N	Second Pixel Negative LVDS differential data input. Channel 3	(4)
39	CH2_3P	Second Pixel Positive LVDS differential data input. Channel 3	
40	CH2_4N	Second Pixel Negative LVDS differential data input. Channel 4	
41	CH2_4P	Second Pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	(1)

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43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	Vin	Power input (+12V)	
49	Vin	Power input (+12V)	
50	Vin	Power input (+12V)	
51	Vin	Power input (+12V)	

Note (1) Reserved for internal use. Please leave it open.

Note (2) Low or Open: VESA Format(default), connect to GND. High: JEIDA Format, connect to +3.3V.

Note (3) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 120 Hz frame rate.
H	Lookup table was optimized for 100 Hz frame rate.

Note (4) LVDS 4-Port Data Mapping

Port	CH of LVDS	Data Stream
1st Port	First pixel	1, 5, 9, ..., 1913, 1917
2nd Port	Second pixel	2, 6, 10, ..., 1914, 1918
3rd Port	Third pixel	3, 7, 11, ..., 1915, 1919
4th Port	Fourth pixel	4, 8, 12, ..., 1916, 1920

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5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2-CN7 (Housing): 51281-1094 (Molex) or Aces 91500-01001

Pin No.	Symbol	Description
1	VLED	Positive of LED String
2	VLED	
3	NC	No Connection
4	NC	
5	NC	
6	N1	Negative of LED String
7	N2	
8	N3	
9	N4	
10	N5	

Note (1) The backlight interface housing for high voltage side is a model 51281-1094, manufactured by Molex or equivalent. The mating header on converter part number is 51281-0994

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5.3 CONVERTER UNIT

CN1(Header): S14B-PH-SM4-TB (JST) or CI0114M1HR0-LA (CvilLux)

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		
11	STATUS	Normal (3.3V) Abnormal (0V)
12	E_PWM	External PWM control signal
13	I_PWM	Internal PWM control signal
14	BLON	Backlight on/off control

Notice:

#PIN 12:PWM Dimming Control (Use Pin 12) : Pin 13 must open.

#PIN 13:Analog Dimming Control (Use Pin 13) : 0V~3.3V and Pin 12 must open.

#Pin 13(I_PWM) and Pin 12(E_PWM) can not open in same period.

CN2 CN4 CN5 CN7 : 51281-1094 (Molex) or Aces 91500-01001

Pin №	Symbol	Feature
1	VLED	Positive of LED String
2	VLED	
3	NC	No Connection
4	NC	
5	NC	
6	N1	Negative of LED String
7	N2	
8	N3	
9	N4	
10	N5	

CN3 CN6 : 51281-1094 (Molex) or Aces 91500-01001

Pin №	Symbol	Feature
1	N5	Negative of LED String
2	N4	
3	N3	
4	N2	
5	N1	
6	NC	No Connection
7	NC	
8	NC	
9	VLED	Positive of LED String
10	VLED	

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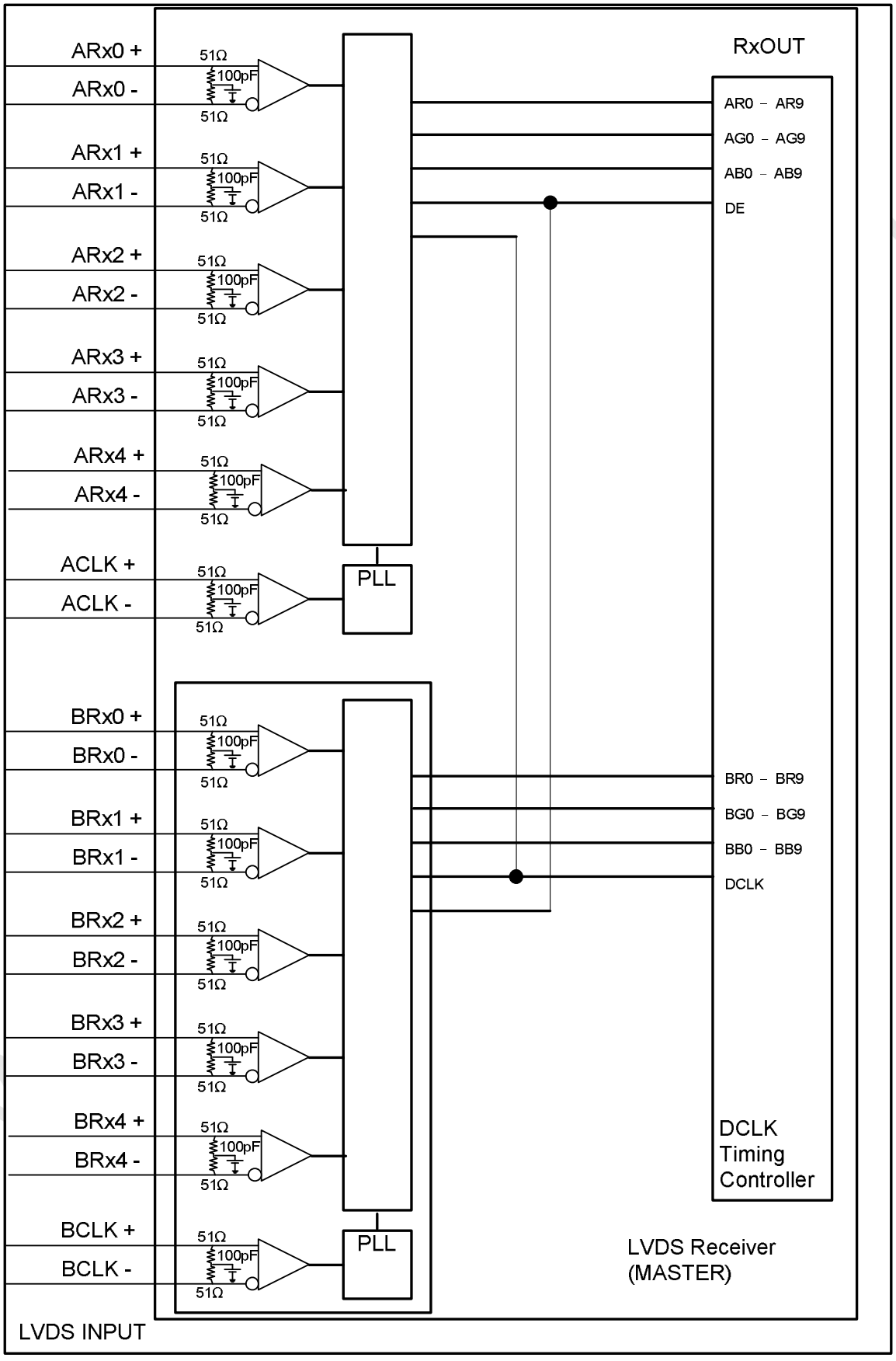
5.4 BLOCK DIAGRAM OF INTERFACE



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AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR9: Third pixel R data

CG0~CG9: Third pixel G data

CB0~CB9: Third pixel B data

DR0~DR9: Fourth pixel R data

DG0~DG9: Fourth pixel G data

DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

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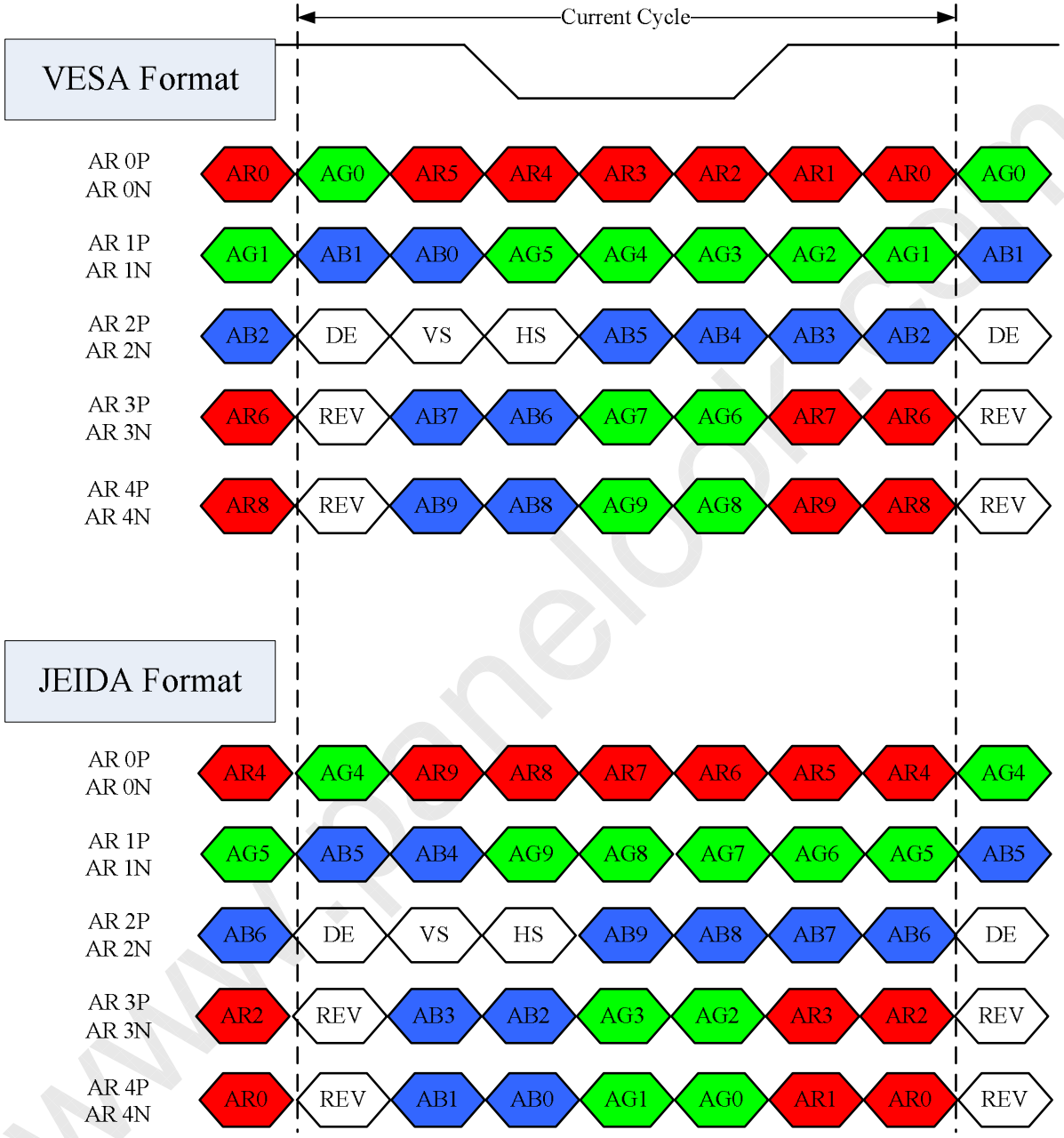
5.5 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

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5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	;	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1

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	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	-	100	-	Hz	(6)
		F_{r6}	-	120	-	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	525	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	—
	Blank	Thb	45	70	95	Tc	—

Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

$$Fclkin(max) \geqq Fr6 \times Tv \times Th$$

$$Fr5 \times Tv \times Th \geqq Fclkin(min)$$

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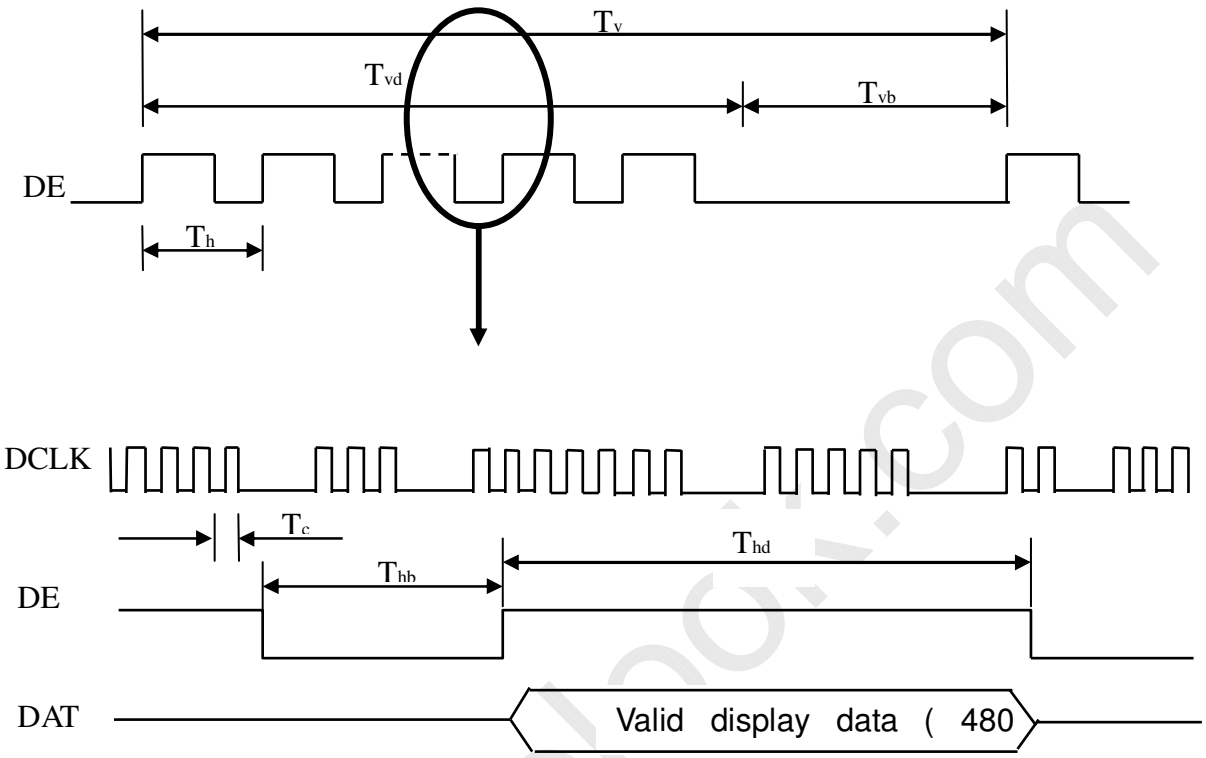
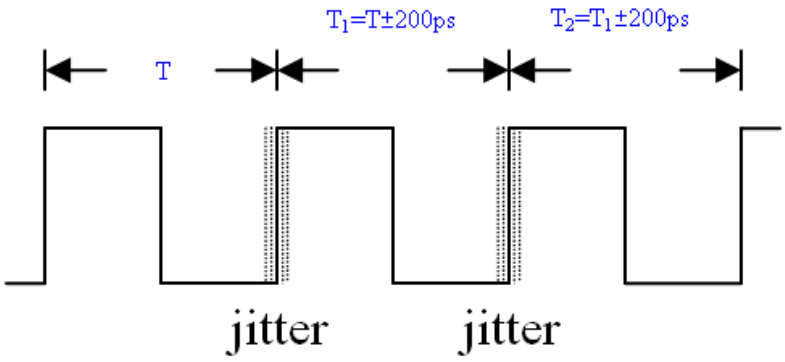
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



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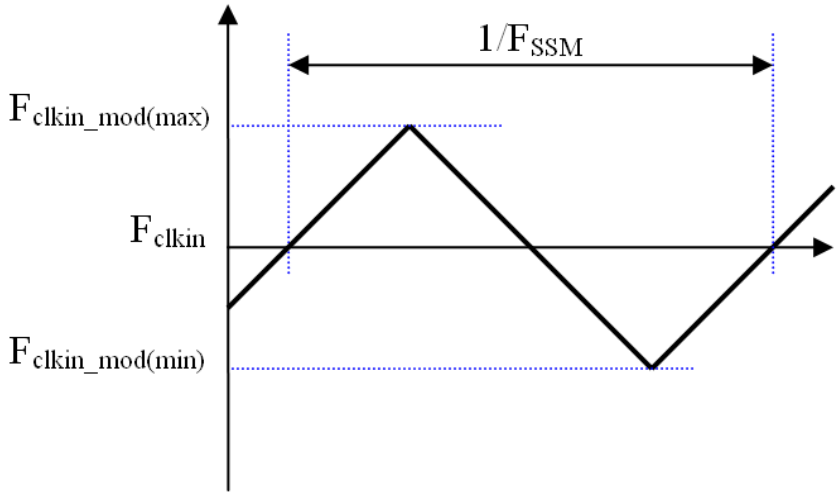
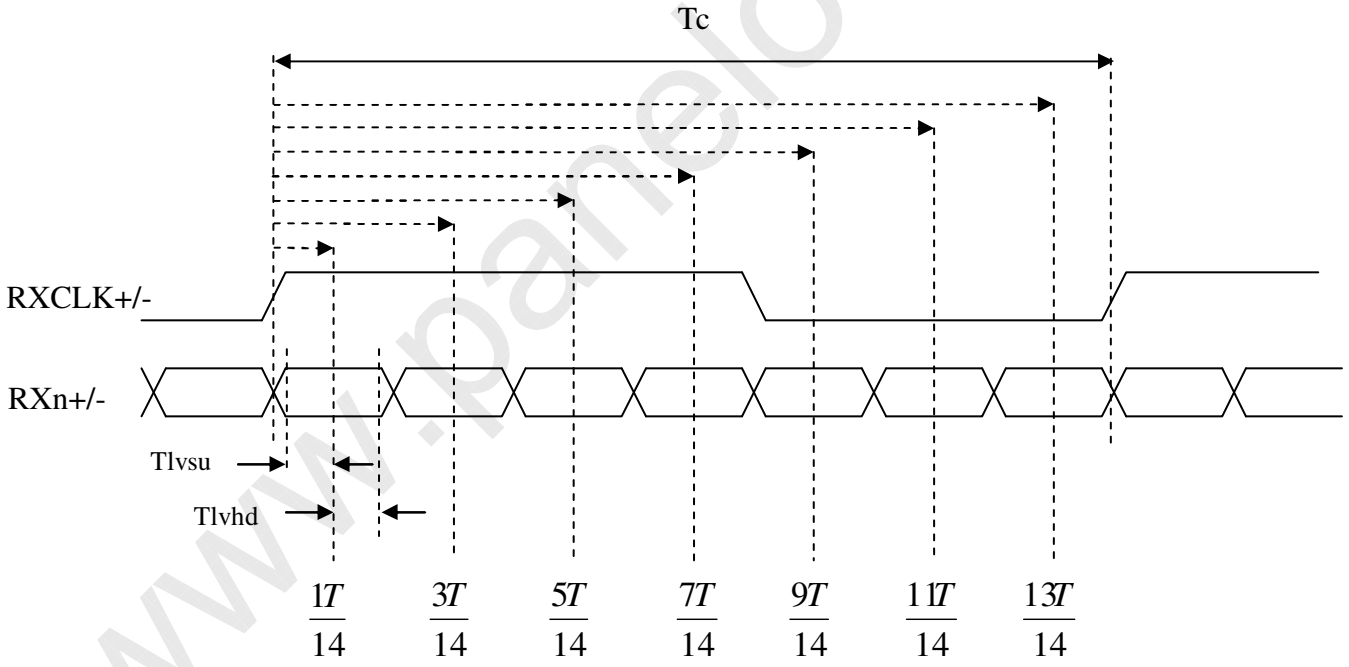
Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) : (ODSEL) = H/L or open for 100/120Hz frame rate. Please refer to 5.1 for detail information

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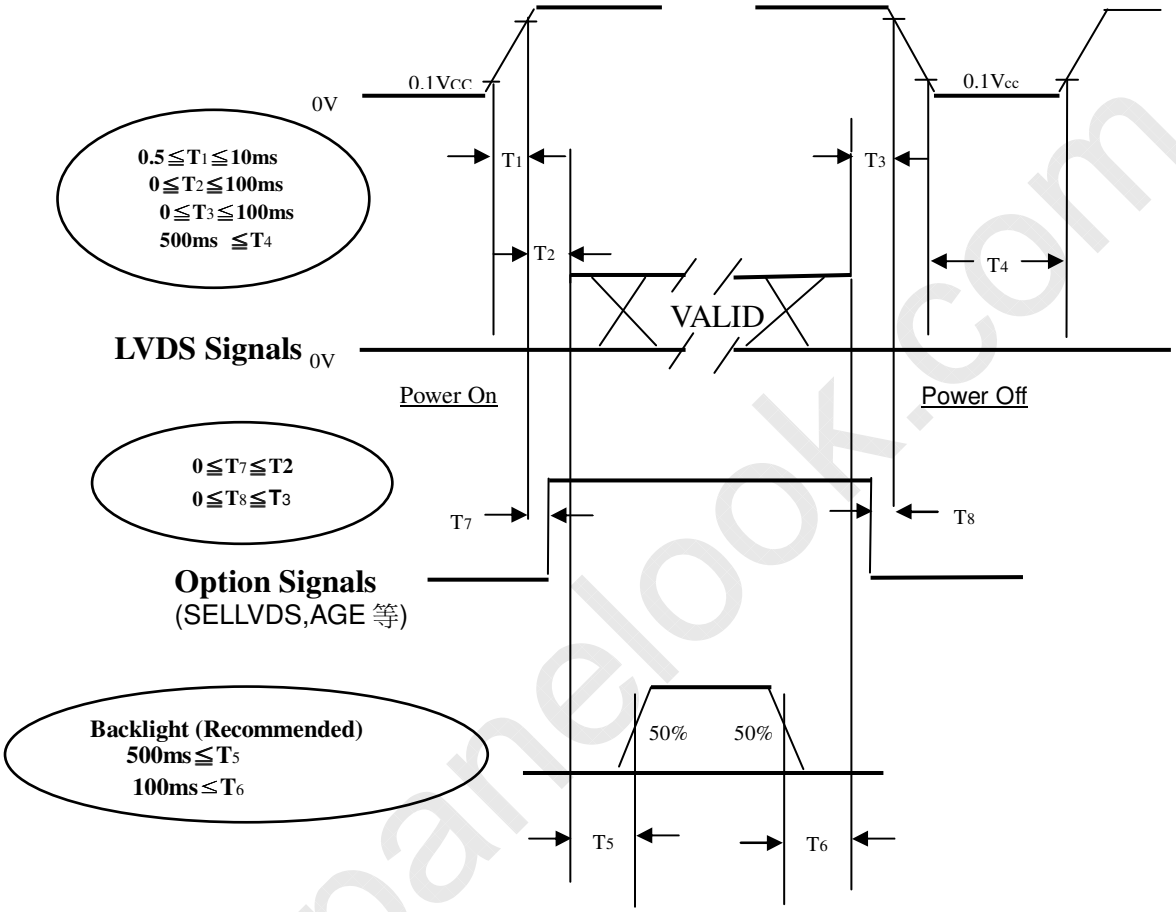
6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note.

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failures.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

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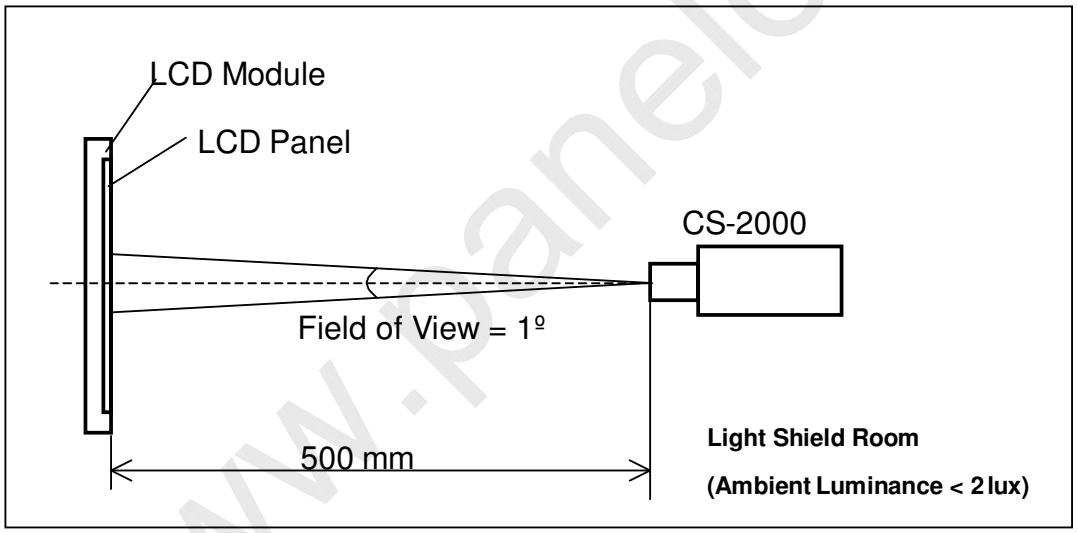
7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	60	mA
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



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7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	3000	4000	-	-	Note (2)
Response Time		Gray to gray		-	4.5	10	ms	Note (3)
Center Luminance of White		LC		360	450	-	cd/m^2	Note (4)
White Variation		δW		-	-	1.4	-	Note (6)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ. – 0.03	0.638	Typ+ 0.03	-	-
		Ry			0.345		-	
	Green	Gx			0.316		-	
		Gy			0.613		-	
	Blue	Bx			0.151		-	
		By			0.051		-	
	White	Wx			0.285		-	
		Wy			0.293		-	
	Color Gamut	C.G		-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	Note (1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Conoscope Cono-80

Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

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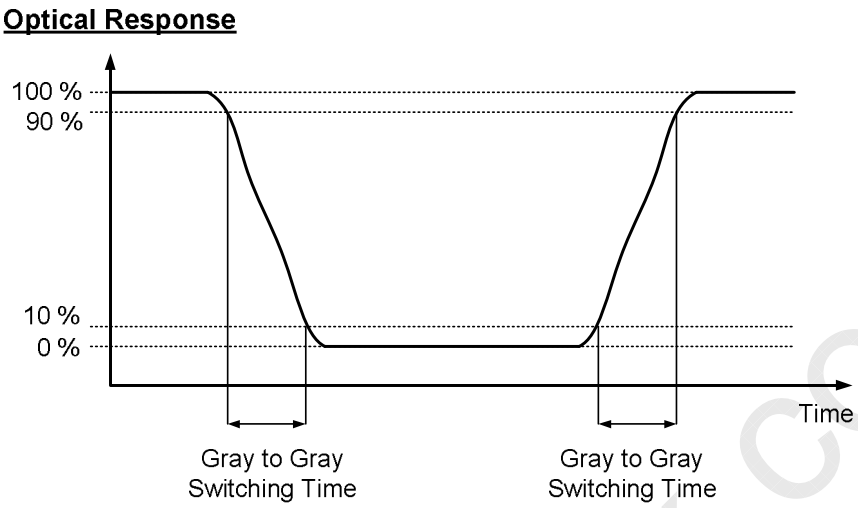
Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other .

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

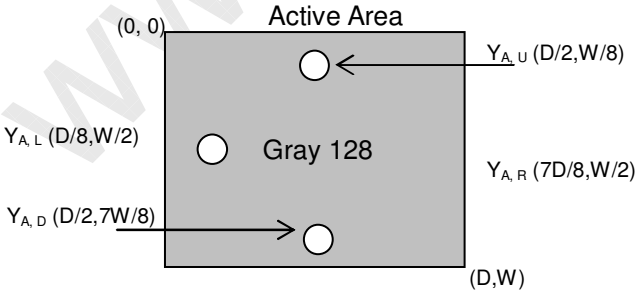
Note (5) Definition of Cross Talk (CT):

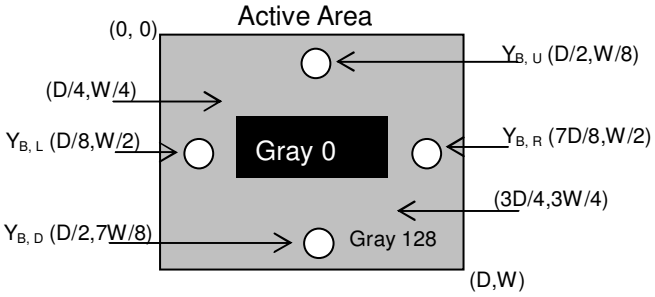
CT = | YB – YA | / YA × 100 (%)

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)





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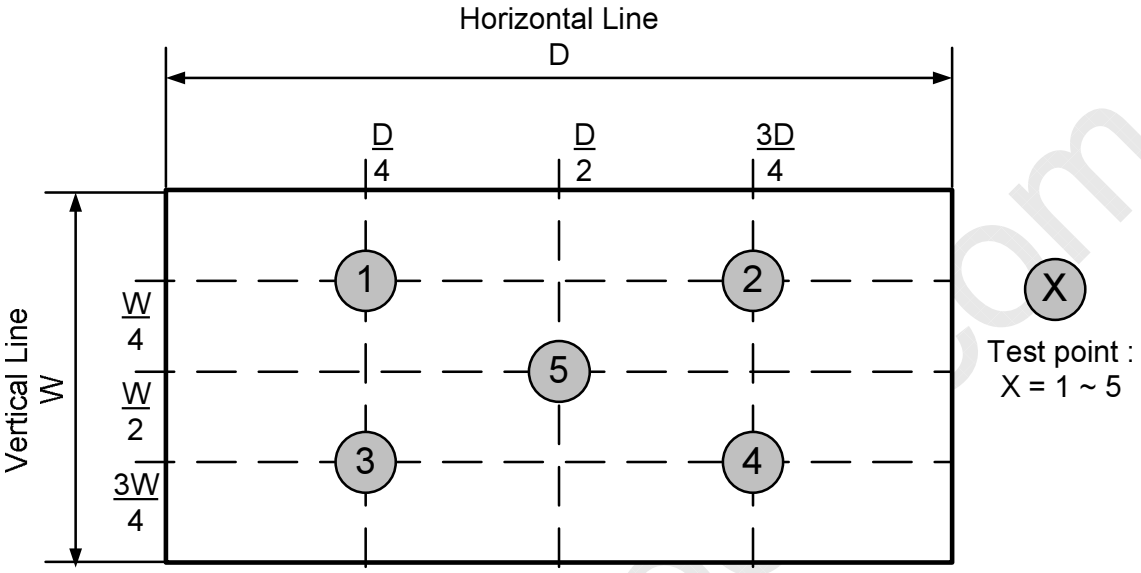
Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



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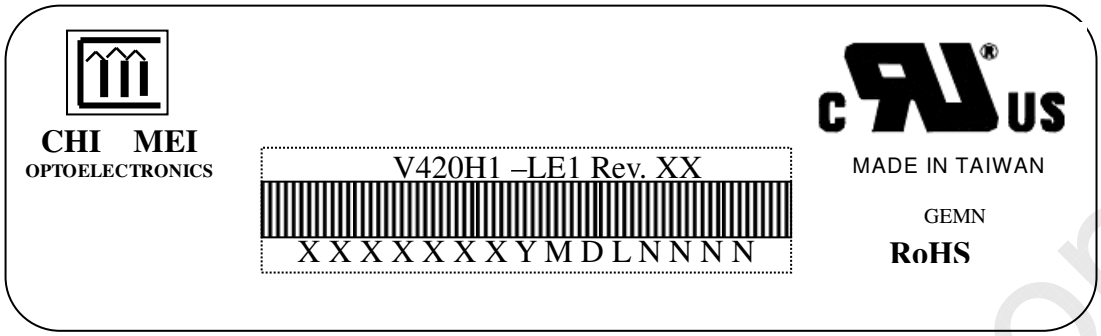
8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

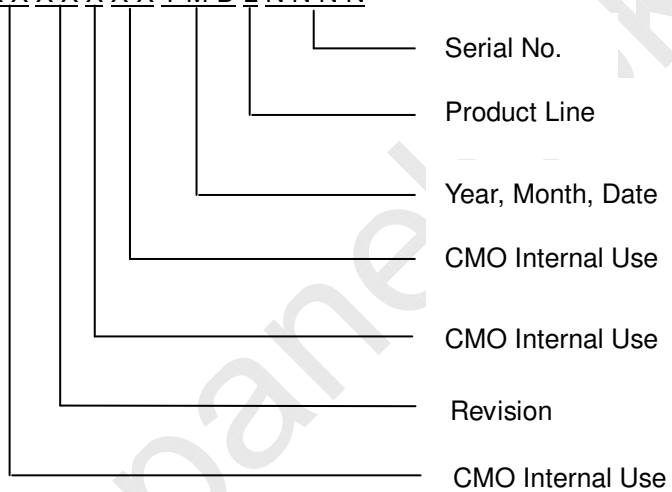
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V420H1-LE1

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

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9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 5 LCD TV modules / 1 Box

(2) Box dimensions : 1085(L)x296(W)x653(H)mm

(3) Weight : Approx. 48 Kg(5 modules per carton)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

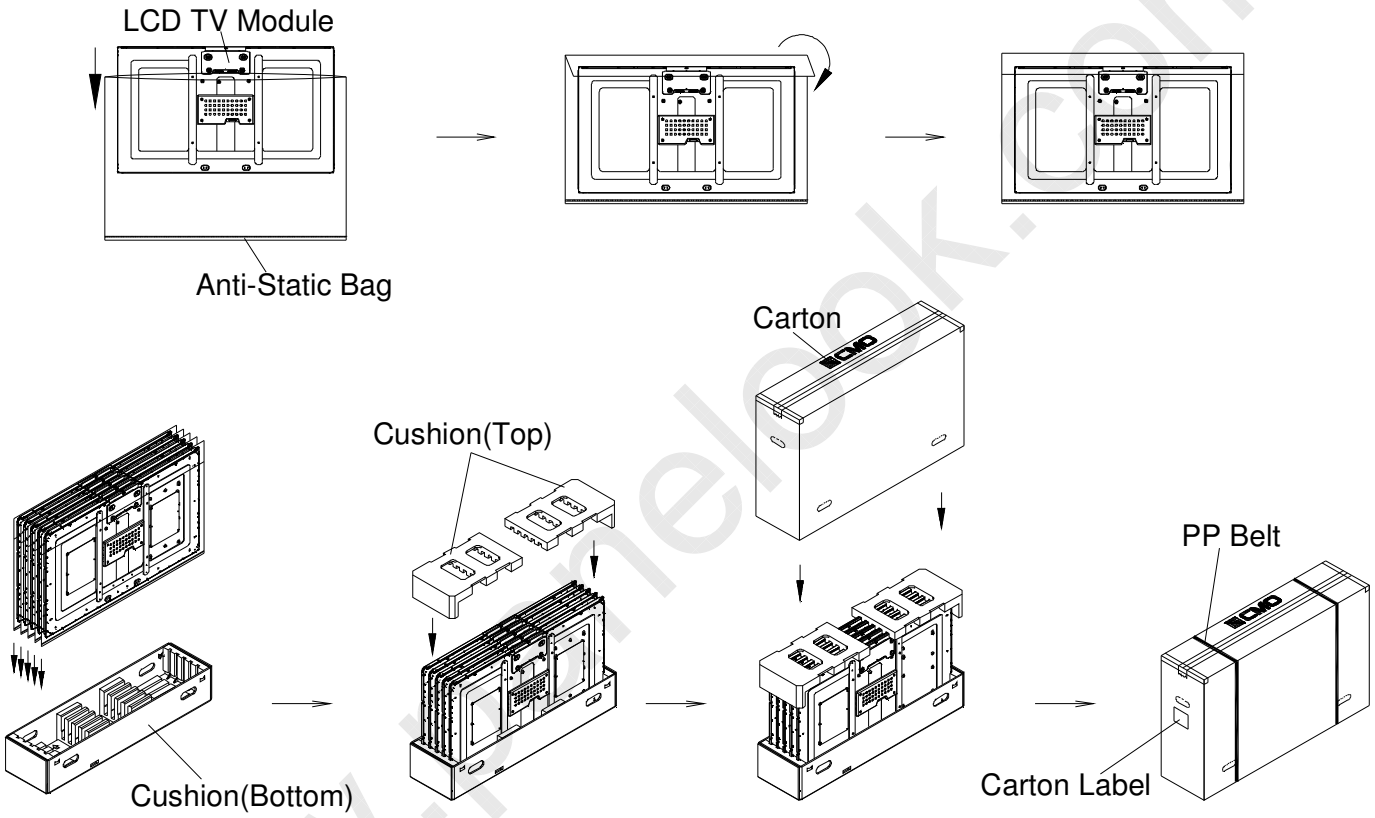

Figure.9-1 packing method

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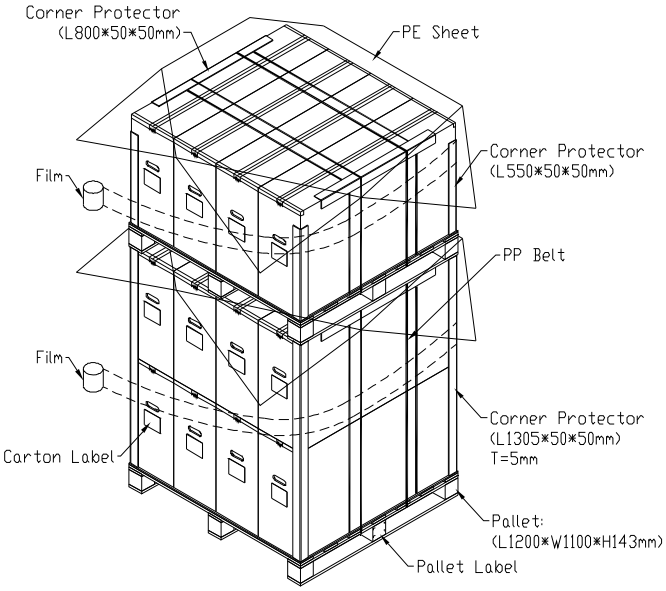
Sea / Land Transportation
(40ft Container)

Air Transportation



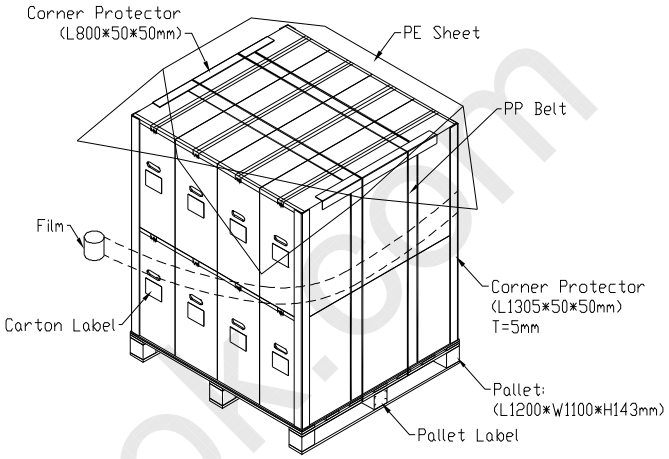


Figure.9-2 packing method

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10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED light bar will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the converter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

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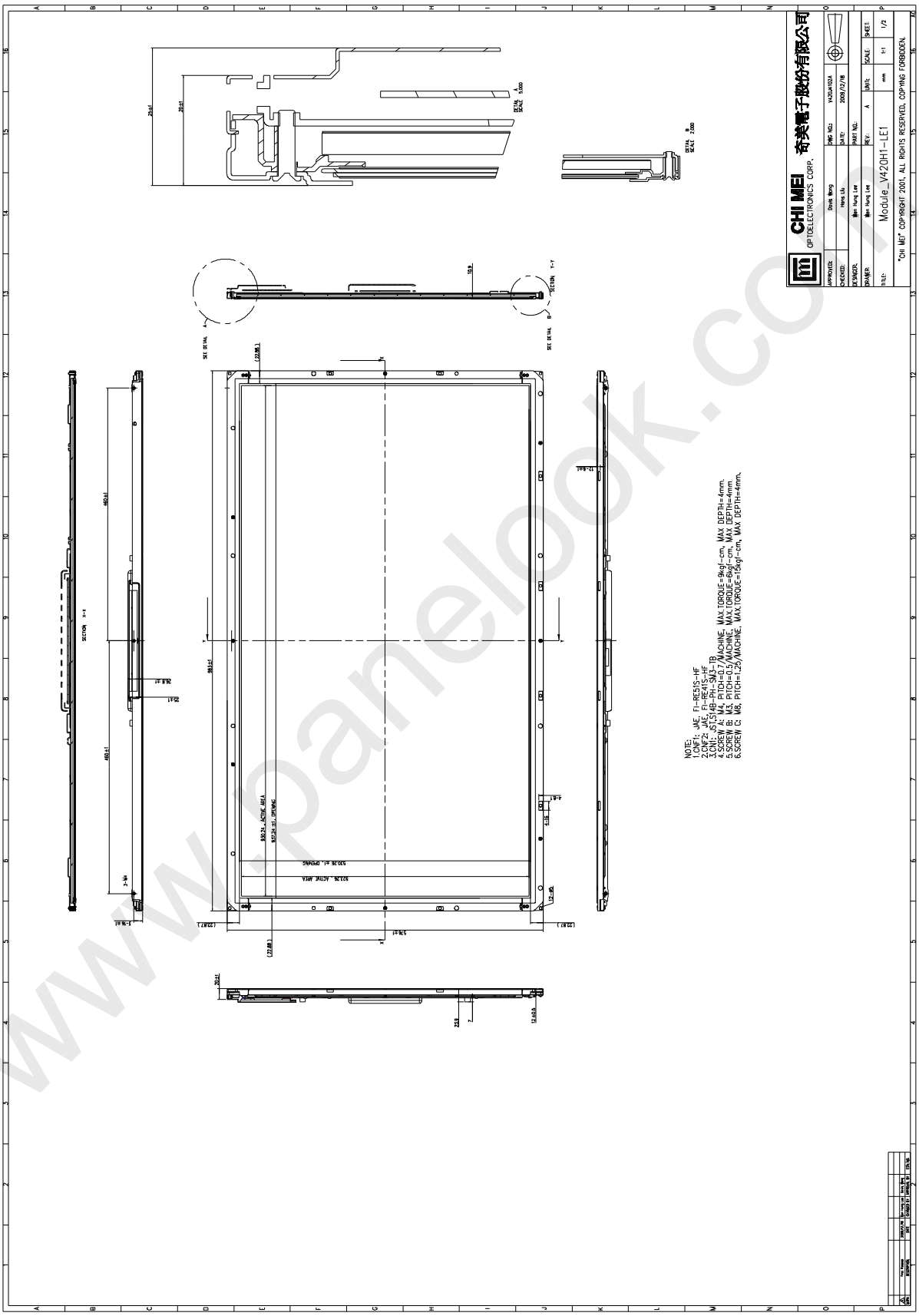
11. MECHANICAL CHARACTERISTICS



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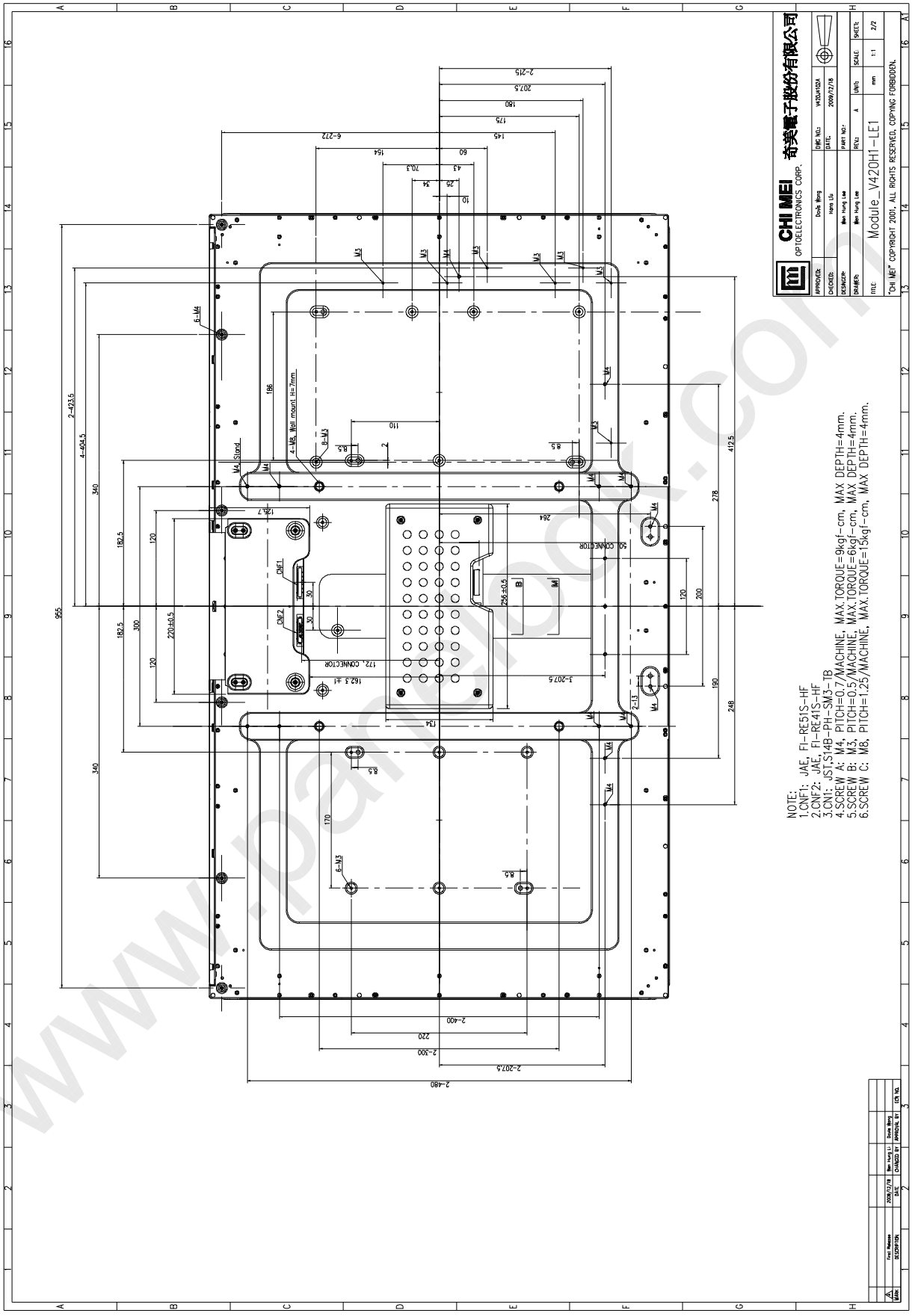

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